Abstract

A MIS transistor, formed on a semiconductor substrate, assumed to comprise a semiconductor substrate (702, 910) comprising a projecting part (704, 910B) with at least two different crystal planes on the surface on a principal plane, a gate insulator (708, 920B) for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part, a gate electrode (706, 930B), comprised on each of said at least two different crystal planes constituting the surface of the projecting part, which sandwiches the gate insulator with the said at least two different planes, and a single conductivity type diffusion region (710a, 710b, 910c, 910d) formed in the projecting part facing each of said at least two different crystal planes and individually formed on both sides of the gate electrode. Such a configuration allows control over increase in the element area and increase of channel width.